AMENDMENTS TO THE DRAWINGS

Replacement Sheet 1, which includes FIG. 1, replaces the original sheet including FIG. 1.

In FIG.1 the previously omitted legend "Prior Art" has been added.

Attachment: Replacement Sheet 1

                     Annotated Sheet Showing Changes

Application No. 10/684,093
Amendment dated March 8, 2005 Reply to Office action of December 16, 2004
Attorney Docket No.: CRU03-0006 (52505-00010)   Express Mail Label: EV66413200US

REMARKS

Claims 1 - 28 are pending in the application. Claims 12 – 19 are allowed. Claims

1, 2, 20 and 21 are rejected. Claims 3 – 11 and 22 – 28 are objected to as being dependent

upon a rejected claim but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims. Applicant

thanks the examiner for allowance of claims 12 -19. For the reasons discussed below,

Applicant respectfully requests allowance of claims 1 – 11 and 20 – 28.

The Rejections under 35 U.S.C. §102

Claim 1 is rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent

No. 5,923,193 to Bloch et al. (hereinafter referred to as "Bloch"). Applicant respectfully

traverses the Examiner's position for the following reasons.

Claim 1 is directed to a signal synchronizing circuit for prohibiting signals

traveling from a first clock domain operating with a first clock to a second clock domain

operating with a second clock when the first clock is not active. The signal

synchronizing circuit includes a detection circuit producing a detection signal

indicating that the first clock is active.

Block teaches an apparatus including a digital data storage element 160

operating in a varying phase clock domain, and a digital data storage element 180

operating in a fixed phase clock domain (FIG. 1). A detect circuit 110 outputs a signal C

to control a data value retention element 170, which further controls the digital data

signal traveling from the digital data storage element 160 to the digital data storage

element 180 (col. 5, line 56 – col. 6, line 5).

The fixed phase clock domain taught by Block is comparable to the second clock

domain disclosed in claim 1 of the present application. In the office action, the

Examiner points out that "Block discloses in figure 1… a second clock domain 180

operating with a second clock B" (page 2, lines 19-20). Since the digital data storage

element 180 operates in a fixed phase clock domain, it is reasonably inferred that the

Examiner regards the fixed phase clock domain comparable to the second clock domain.

Moreover, the fixed phase clock domain and the second clock domain are comparable

in the sense that they are the clock domains at the signal-receiving end. In Block,

signals travel from the digital data storage element 160 operating in a varying phase

clock domain to digital data storage element 180 operating in a fixed phase clock

domain (FIG. 1). In claim 1 of this application, signals travel from a first clock domain

to a second clock domain. The fixed phase clock domain and the second clock domain

are at the signal receiving end, as opposed to the varying phase clock domain and the

first clock domain.

Bloch fails to disclose the detection circuit as described in claim 1. In Block, the

detect circuit 110 detects a change in state for the clock signal for the fixed phase clock

domain (FIG.1 and col. 6, lines 2 – 5). Since the fixed phase clock domain is comparable

to the second clock domain, the detect circuit 110 detects a change in state for the

second clock domain, not the first clock domain. However, the present invention as

described in claim 1 calls for detecting that the first clock operating in the first clock

domain is active. In other words, the claimed detection circuit is not used for detecting

a change in state for the second domain. As such, Bloch teaches a detection mechanism

fundamentally different from the claimed invention, and can not anticipate the same.

Accordingly, claims 2 – 11 depending on the independent claim 1 are patentable over

Bloch as well.

Claim 20 is directed to a method that includes a step of detecting that the first

clock operating in the first clock domain is active. For the same reasons discussed

above, claim 20 is not anticipated by Bloch. Accordingly, claims 21 – 28 depending on

the independent claim 20 are patentable over Bloch as well.

CONCLUSION

Applicant has made an earnest attempt to place this application in an allowable form. In view of the foregoing remarks, it is respectfully submitted that the pending claims are drawn to a novel subject matter, patentably distinguishable over the prior art of record. The Examiner is therefore, respectfully requested to reconsider and withdraw the outstanding rejections.

Should the Examiner deem that any further clarification is desirable, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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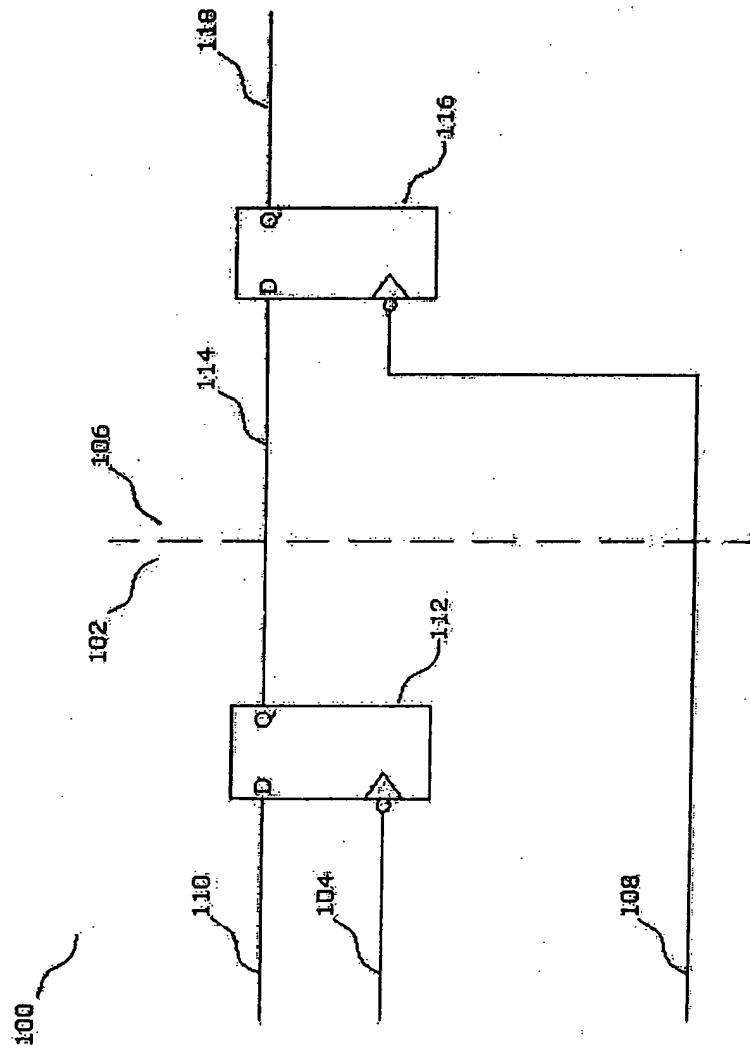Facsimile: (415) 882-8220

CRU03-06 2nd D-Res to 1st OA.doc

U.S. Patent Appln for
SYNCHRONIZER APPARATUS FOR SYNCHRONIZING DATA FROM ONE
CLOCK DOMAIN TO ANOTHER CLOCK DOMAIN
Inventor(s): Richard L. Duncan
Atty Docket No.: N1194-00007
Annotated Sheet Showing Changes

FIG. 1 (PRIOR ART)